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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,069	07/23/1999	PETER WOHL	SNSY-A1998-0	3639

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SYNOPSYS, INC. C/O BEVER, HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE, CA 95110-1017

EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	11

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION: Final (second office action after RCE)

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS
2. First named inventor is: WOHL
3. Claims 1 (thrice amended), 2, 3 (amended), 4-12, 13 (currently amended), 14, 15 (currently amended), 16-24, 25 (currently amended), 26 (currently amended), 27 (currently amended), 28-35, and 36 (currently amended) are pending.
4. This action is in reply to Applicant's Amendment received 6/9/03.

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5. **Cheng** refers to Gate-Level Test Generation for Sequential Circuits, by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.
6. **Beausang'771** refers to US Patent 5,696,771.
7. **MS Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.

Applicant's Remarks

8. ROM AMENDMENTS. Applicant has substantially amended the independent claims to treat ROM differently from non-ROM. The Examiner finds these amendments well supported in the original disclosure at Specification page 5 line 4 "does not require re-coding for most ROMS", and page 15 line 5 "behavioral descriptions of ROMs ... are used directly". Thus, the amendments are not new matter.
9. The Examiner emphasizes this point because these ROM limitations are potentially patentable. The Examiner has not found these limitations explicitly in the prior art. The Examiner rejects (below) these limitations partially on the basis of MPEP 2144.04(II)(A) which states that "Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired", and motivated by Cheng to ignore circuit delays.

10. **The reasons for treating ROM differently from non-ROM are important. If Applicant provides a good explanation why ROM and non-ROM are treated differently, and a related good explanation why this different treatment would not be obvious to one of ordinary skill in the art, then said explanations would be given substantial weight in determining patentability.**
11. BEAUSANG. Applicant unpersuasively asserts that it would not be obvious to modify Beausang in view of Cheng, because Beausang "could not be optimized" without timing information or physical layout information. Note that Beausang Abstract states "maintaining specified optimization (e.g., area and/or timing) constraints". Thus, timing information could be eliminated from Beausang if only area optimization was desired, and similarly area information could be eliminated from Beausang if only timing optimization was desired.
12. Note that the term "e.g." is defined by Black's Law Dictionary Sixth Edition as "An abbreviation of *exempli gratia*. For the sake of an example." Thus, Beausang does not necessarily require timing or physical layout information, but rather these are merely free (*gratia*) examples (*exempli*) of "maintaining specified optimization".
13. ATPG MEMORY PRIMITIVES. Applicant unpersuasively asserts that Beausang does not disclose the ATPG memory primitives. One of ordinary skill in the art would interpret Beausang as broadly disclosing primitives, including ATPG memory primitives.
14. Beausang must be interpreted in the light of what one of ordinary skill in the art would know. MS Dictionary defines "logical" as "Based on true and false alternatives as opposed to arithmetic calculation of numeric values... Boolean algebra", and defines "primitive" as "In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants". Thus, Beausang broadly teaches logical primitives, including memory primitives and including pluralities of primitives.

35 USC § 112-Second Paragraph-indefinite claim-WITHDRAWN

15. The prior 35 USC 112 rejections are withdrawn due to Amendments.

Claim Interpretation

16. After substantial discussion, the Applicant and Examiner are agreed that three distinct types of memory models are used:

    simulation memory model (behavioral HDL),

simplified behavioral memory model (using proper subset of behavioral HDL), and structural memory model (plurality of ATPG memory primitives).

17. Based upon the amendments, note that the structural memory model may be based upon either the simulation memory model (for ROM), or based upon the simplified behavioral memory model for (non-ROM).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

Determining the scope and contents of the prior art.

Ascertaining the differences between the prior art and the claims at issue.

Resolving the level of ordinary skill in the pertinent art.

Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable.

20. Claim 1 (thrice amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of MPEP 2144.04(II)(A) Routine Expedient of omission of an element and its function, and Official Notice, and Cheng.

21. Claim 1 (twice amended) is an independent method claim with 5 steps, labeled A-E by the Examiner.

22. A-**accessing a simulation model of said memory, from a simulation library stored in a computer system memory, wherein said simulation model is described in a behavioral hardware description language** is disclosed by Beausang'771 at FIG 8 element 605 "HDL DESCRIPTION". Note that HDL stands for "hardware description language". The Examiner hereby takes official notice that it is common knowledge to create simulation models of memories using hardware description languages (such as VHDL or Verilog), and to store

these models in a simulation library in a computer system memory, and to access this simulation model.

23. B-**if said memory is a read only memory (ROM), then proceeding directly to translation** is disclosed by Beausang`771 at FIG 8
24. element 605 "HDL DESCRIPTION" and element 615 "COMPILE..." and element 655 "ATPG AND FORMAT". Note that Beausang'771 is applicable to logical elements in general, including ROM.
25. D-**automatically translating said simulation model or simplified behavioral model of said memory into said structural model of said memory, wherein said structural model comprises a plurality of ATPG memory primitives** is disclosed by Beausang`771 at FIG 8 element 605 "HDL DESCRIPTION" and element 615 "COMPILE..." and element 655 "ATPG AND FORMAT". Note that the term "automatically" is not given patentable weight in this limitation because *In re Venner*, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." See MPEP 2144.04(III).
26. Beausang`771 does not explicitly disclose the remaining limitations.
27. C-**if said memory is other than a ROM, then generating a simplified behavioral model of said memory by re-describing said simulation model of said memory with a predefined proper subset of said behavioral hardware description language** is Routine Expedient. MPEP 2144.04(II)(A) states that "Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired". Here, for example, a proper subset of said behavioral HDL may be created by eliminating timing information when "not desired or required" according to MPEP 2144.04(II)(A). As a second example, a second proper subset of said behavioral HDL may be created by eliminating layout information when "not desired or required" according to 2144.04(II)(A). Thus, this second step is disclosed by legal precedent regarding Routine Expedient. See *Ex parte Wu,* 10 USPQ2d 2031, 2032 (Bd. Pat. App. & Inter. 1989), and see *In re Larson,* 340 F.2d 965, 144 USPQ 347, 350 (CCPA 1965) which states "If this additional features (sic) is not desired, it would seem a matter of obvious choice to eliminate it and the function it serves". Further, note that MPEP 2144.04(II)(B)

states "the omission of an element and retention of its function is an indicia of nonobviousness". However, the function is not retained in this limitation, so there is no indicia of nonobviousness.

28. E-**storing said structural model in said computer system memory** is disclosed by Official Notice that it is common knowledge in the art to store structural models in computer system memories.
29. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Routine Expedient and Official Notice and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a proper subset (Routine Expedient) to create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.
30. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of MPEP 2144.04(II)(A) Routine Expedient of omission of an element and its function, and Official Notice, and Cheng.
31. Claim 2 depends from claim 1 (thrice amended), with one additional limitation.
32. Beausang'771 does not expressly disclose the additional limitation.
33. **simplified behavioral model excludes timing information** is disclosed by Routine Expedient, as discussed above in Claim 1 (twice amended).
34. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Routine Expedient and Official Notice and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a proper subset (Routine Expedient) to create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in

order to easily access these models for various computer simulations to test the circuit design.

35. **Applicant Remarks page 8, regarding claim 2 and claim 3 (amended).**
36. Applicant persuasively asserts that Cheng's structural models do appear to contain timing and/or layout information, because Cheng explicitly discloses "ignoring" delays. Applicant proposes that Cheng's delays result from different signal propagation paths, and that Cheng retains and utilizes timing and/or layout information. The Examiner is not certain exactly which "circuit delays" Cheng is ignoring. Cheng at page 406 states "We focus on the methods that are based on gate-level circuit models". Thus, these delays appear to be at least dependent upon the timing and/or layout information. Therefore, Cheng at page 407 appears to retain certain information, but ignores this information (or at least the delays that results from it) during a "potential test".
37. Please note that Cheng is not used in this rejection for disclosing the specific limitation of excluding timing and/or layout information from a structural model. Cheng is used only for motivation. Cheng specifically discloses performing some tests using ATPG methods while ignoring delays. Thus, Cheng serves as motivation for combining the Routine Expedient of omission of an element and its function (delays or timing/layout related information) with the "HDL" and "ATPG" of Beausung'771. In other words, Cheng discloses that it is well known in the art that delays or timing/layout related information is sometimes not desired. Note that *In re Larson,* 340 F.2d 965, 144 USPQ 347, 350 (CCPA 1965) states "If this additional features (sic) is not desired, it would seem a matter of obvious choice to eliminate it and the function it serves".
38. Claim 3 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of MPEP 2144.04(II)(A) Routine Expedient of omission of an element and its function, and Official Notice, and Cheng.
39. Claim 3 depends from claim 2, with one additional limitation.
40. Beausang'771 does not expressly disclose the additional limitation.
41. **said simplified behavioral model excludes physical layout information contained in said simulation model of said memory** is disclosed by Routine Expedient, as discussed above in Claim 1 (twice amended).

42. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Routine Expedient and Official Notice and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a proper subset (Routine Expedient) to create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.
43. Claims 4-12 all depend from Claim 1 (thrice amended), and are rejected for the same reasons as Claim 1 (thrice amended) above, in addition to the reasons previously stated in the prior Office Action, mailed 5/9/02. There have been no amendments to claims 4-12.
44. Claims 13-24 are "computer readable medium" claims with the same limitations as "method" Claims 1-12, and therefore are rejected for the same reasons.
45. Note that claim 13 (currently amended) has been amended to have the same limitations as Claim 1 (thrice amended). Similarly, Claim 15 (currently amended) has been amended to have the same limitations as Claim 3 (amended). Thus, the "computer readable medium" claims mirror the limitations of the "method" claims.
46. Claims 25-36 are "computer controlled electronic design automation systems" (apparatus) claims with the same limitations as "method" Claims 1-12, and therefore are rejected for the same reasons. Note that Claim 25 (currently amended) has been amended to have the same limitations as Claim 1 (thrice amended). Similarly, Claim 26 (currently amended) has been amended to have the same limitations as Claim 2 (original). Similarly, Claim 27 (currently amended) has been amended to have the same limitations as Claim 3 (amended). Thus, the "computer controlled electronic design automation" (apparatus) claims mirror the limitations of the "method" claims.

Response to Amendments or new IDS-FINAL OFFICE ACTION

47. Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A

shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Patentable material

48. The Examiner has rejected the limitations containing simplified behavioral memory models for non-ROM because of MPEP 2144.04(II)(A), which states that "Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired".
49. However, if Applicant provides a good explanation why ROM and non-ROM are treated differently, and a related good explanation why this different treatment would not be obvious to one of ordinary skill in the art, then said explanations would be given substantial weight in determining patentability.
50. The Examiner suggests that an interview may be an efficient way to explore and clarify these issues.

Conclusions

51. All pending claims are rejected against prior art under 35 USC 103.
52. The prior indefiniteness rejection has been withdrawn.
53. No additional prior art has been cited.

Communication

54. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.
55. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:
56. (703) 746-7238 --- for communications after a Final Rejection has been made;
57. (703) 746-7239 --- for other official communications; and

58. (703) 746-7240 --- for non-official or draft communications.

59. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER